IM0418

Acousto-Optic Modulator Driver

Including: Modulator Alignment
AOM740-H

Instruction Manual

RFA741 Series
Digital Modulation, Dual Frequency
Remote Power Level Control

Models -

RFA741 : 40MHz / 50.7MHz, 180W output

Options **–xxx**, combinations possible.

- BR : Brass water cooled heatsink

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1. GENERAL

Key Features:

- 24Vdc, water cooled high power amplifier
- RF output >150W at 40.00MHz, and >150W at 50.67MHz
- RF rise/fall time < 400/100nsec at 150W
- High Speed Digital ON:OFF modulation
- Modulation ON level is defined by two methods for each frequency
  - Digitally programmed potentiometer stack
  - Manual adjustment potentiometer.
- Digital potentiometers programmed via buffered I2C interface
- Opto-isolated PLC compatible inputs on POT select and RF enable inputs.
  (Response time < 1msec)
- Tri colour LED status indicator
- High VSWR shut-down protection

The RFA741 Combined Driver and Power Amplifier is a fixed dual frequency RF power source specifically designed to operate with the AOM740- series of acousto-optic high power modulators
A block diagram of the driver is shown in Figure 3. The center frequencies are determined by free-running quartz-crystal oscillator. The frequency is accurate to within ± 25ppm and the stability is better than ± 25ppm. A high-frequency, diode ring modulator provides high speed amplitude modulation of the RF carrier. The peak RF power level for each frequency is set by a multi-turn manual potentiometer or by digitally controlled potentiometers.
The prime frequency of 40MHz provides the active “ON” laser output beam. The dummy frequency of 50.67MHz is applied in the “OFF” condition and is used to provide a constant thermal load to the AOM.

2, CONTROL

Two inputs directly control the RF output; *Gate* and *Freq Modulation*.

The Gate response time (tgm, fig1) is approximately 1msec

The RF Frequency Modulation response time is < 50nsec

The relationship between the driver control inputs, the RF waveform and AO response is shown below.

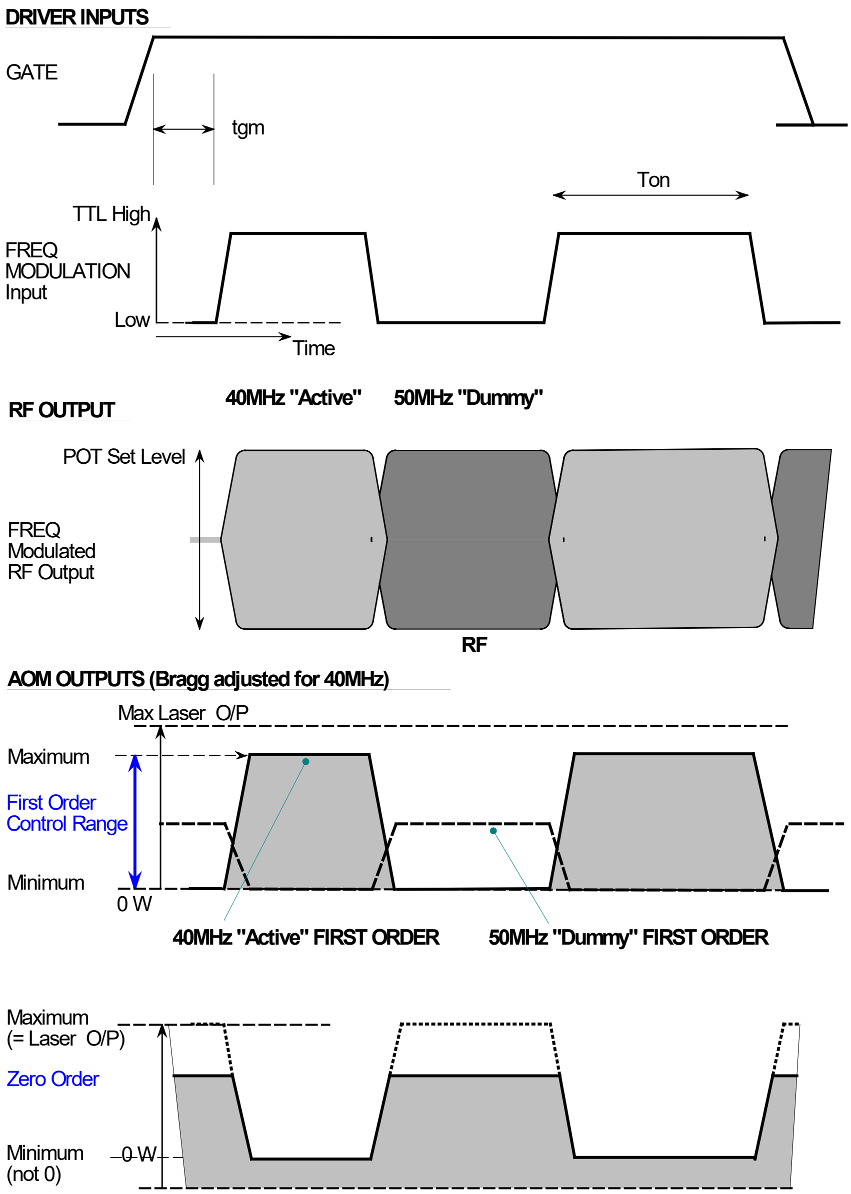

Figure 1: Typical Digital Modulation Waveforms

Gate (active high enables the RF amplifier)

PLC compatible opto-isolated input

Default condition is RF Off.

A high level (5V < V < 24V) will gate the RF **ON**.

A low level (0V < V < 4V), or not connected will gate the RF **OFF.**

Digital Modulation (active high)

Provides high speed frequency selection of the RF output.

A TTL high level will select 40.00MHz (Main 1st order beam "**ON")** .

A TTL low level will select 50.67MHz (Main 1st order beam "**OFF")** .

The amplitude level for either frequency is defined by the selected RF power adjustment POT.

RF Power Adjustment (POT set level)

The maximum RF power limit is set by one of two methods. The method is selectable by the user.

a) A manual adjust multi-turn potentiometer 'PWR ADJ' for each frequency.

Maximum RF power = fully clockwise

or

b) A quad 256 step digital potentiometer configured to give independent power control for 40 and 51.7MHz levels with common variable end limits

All 4 channels are used for power level control. RDAC0, RDAC1, RDAC2 and RDAC3 (see AD5254 data sheet). Levels are set remotely via an I2C compatible serial connection. The slave address for the digital I2C potentiometer is at 0101100. (AD0 = AD1 = 0)

DC Power

A low impedance DC power supply is required. The operating voltage is +24Vdc only at a current drain of approximately < 18A. The external power source should be regulated to ± 2% and the power supply ripple voltage should be less than 200mV for best results. Higher RF output power is achieved at 28Vdc.

2.1 **<u>Thermal Interlocks</u>**

The AOM and Driver are fitted with thermostatic switches which will switch open circuit if a predetermined temperature is exceeded. These thermal interlocks will reset once the AO device and / or RF driver are cooled below this temperature.

- The driver thermal switch over-temperature threshold is 50deg C
- The AOM740-H series thermal switch over-temperature threshold is 32deg C

The hysterisis of the thermal switches is 7-10deg C.
Once in a fault state the coolant temperature may need to be reduced to reset the thermal switches.

Precautions

TTL digital input levels must not exceed 7 volts

PLC logic input levels must not exceed 24 volts

<u>Water cooling is mandatory.</u>
<u>The heatsink temperature must not exceed 70°C.</u>
<u>Corrosion inhibitor should be added to the cooling water</u>

SERIOUS DAMAGE TO THE AMPLIFIER MAY RESULT IF THE TEMPERATURE EXCEEDS 70°C. SERIOUS DAMAGE TO THE AMPLIFIER MAY ALSO RESULT IF THE RF OUTPUT CONNECTOR IS OPERATED OPEN-CIRCUITED OR SHORT-CIRCUITED.

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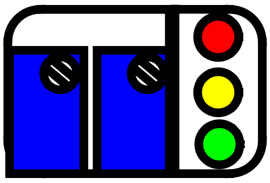
2.2 **LED Indicator and Monitor outputs**

The front panel tri-colour LED indicates the operating state.



(RF PWR ADJ) 51MHz 40MHz LED

RED

The top LED will illuminate RED when there is a poor VSWR load (High reflected RF power fault).

Normal condition is OFF

A fault signal is triggered when the reflected RF power exceeds approximately 50% of the average forward power for more than 1 second. This fault is latching and the driver is disabled (RF power will go to zero). This fault can occur if the RF connection between the AOM and driver is broken.

Resetting

Once the fault condition is corrected, it will be necessary to reset the driver.

1) Turn the DC power OFF and ON

or

2) Press momentary RESET button on driver located to right to the D-type

YELLOW

The middle LED will illuminate YELLOW, when the RF outputs are live and provided that

a) the Gate duty cycle is more than 20% (approx).

b) the RF average power is > 30W (approx)

Normal condition is ON, but may be OFF if the above conditions are not met

GREEN

The lower LED will illuminate GREEN when the following signal are all true:

1) RF DC power is applied and

2) Interlocks are valid and

3) GATE input is high.

Normal condition is ON

LEDS Off

The GREEN and/or YELLOW LED's will not illuminate if :

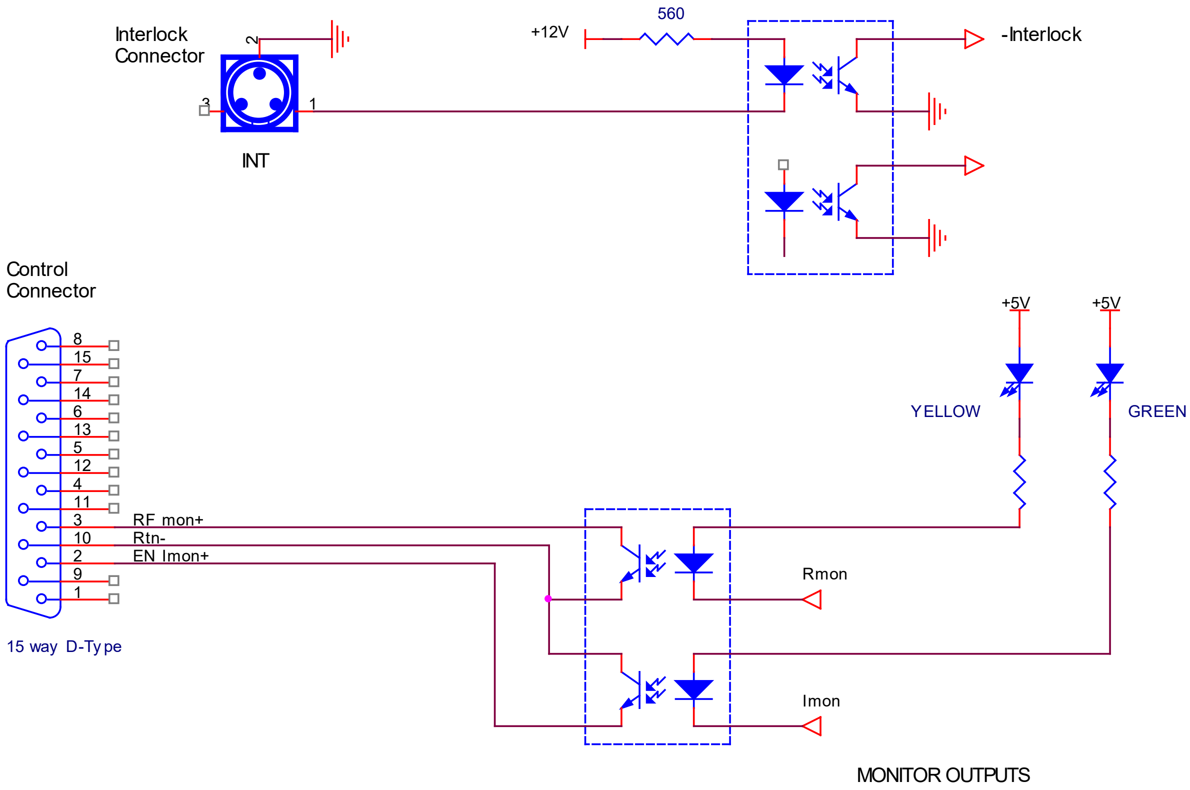
a) the internal driver thermal interlock switch is open (Over temperature fault)
b) the AOM thermal interlocks switch is open (Over temperature fault)
c) the AOM thermal interlock is not connected to the driver interlock input
d) the DC supply is off.

The RED LED should be OFF

Monitor Outputs

The status of the YELLOW and GREEN LEDS is available at the D-type connector

These outputs are opto-isolated .



"Enabled" = low impedance between pins 2 and 10 = Green LED ON

"RF Active" = low impedance between pins 3 and 10 = Yellow LED ON

3. INSTALLATION AND ADJUSTMENT

The basic set-up below is described using the manual RF power limit adjustment.

The remote power adjustment is described from 3.15 onwards. The driver will default to manual adjustment unless the remote power adjustment is selected,

3.1 Connect cooling water to the RFA741 at a minimum flow of 2.0 litres/minute at < 20 deg.C. Refer to Figure 2. Use of a Corrosion inhibitor is strongly advised.

Connect cooling water to the AO device.

Due to the high RF power dissipated in the AO modulator, it is paramount that the device is operated only when water cooling is circulating.

For optimum AO performance ensure the flow rate is more than 2 litres/minute at < 20 deg.C

3.2 With no DC power applied, connect the + 24V DC in to the screw terminals of the filtered terminal. DO NOT APPLY POWER.

3.2 Connect the TNC output RF connector to the acousto-optic modulator TNC RF input. (or a 50Ω RF load, if it is desired to measure the RF output power).

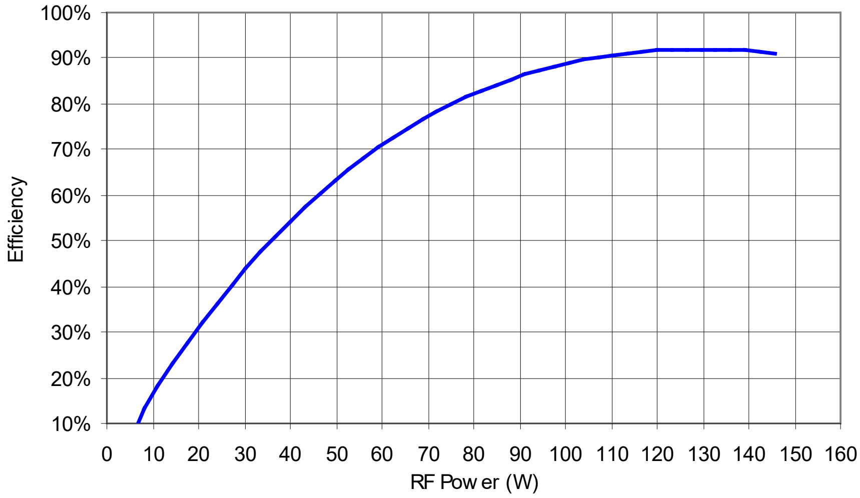
3.4 Connect the Interlock of the acousto-optic modulator (mini 3-pin snap connector) to the RF driver “INT” input (mini 3-pin snap connector). Connect pin 1 to pin 1 and pin 2 to pin 2.

If the temperature of the modulator exceeds 32ºC or the internal driver temperature exceeds 50ºC then the interlock connection becomes open circuit, disabling the RF output. An LED indicator illuminates when the Interlocks are closed and the RF is enabled. In addition, a open drain ‘interlock valid’ signal output is provided on pin 2 of the D-type connector for remote monitoring purposes.

3.5 Adjustment of the RF output power is best done with amplifier connected to the acousto-optic modulator. When shipped, the Amplifier maximum output power is set to approx 100W selecting the manual PWR ADJ pot and 120W for the digital pots.

The optimum RF power level required for the modulator to produce maximum first order intensity depends on the laser wavelength and AOM aperture height. This value is called “Psat”. **Applying RF power in excess of this optimum level will cause a decrease in first order intensity, increase thermal dissipation and make accurate Bragg alignment difficult.** It is therefore recommended that initial alignment be performed at a low RF power level.

A typical relationship between RF drive and efficiency for a correctly aligned AOM740-H at 10.6um is illustrated below.



3.6 Locate the PWR ADJ access holes on the driver end plate.
The 40MHz RF Power adjuster is closest to the LED stack

3.7 With an insulated alignment tool or screwdriver rotate both PWR ADJ potentiometers fully anti-clockwise (CCW) i.e. OFF, then clockwise (CW) approx 5 turns.

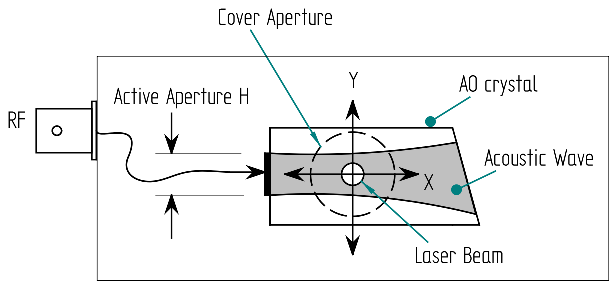
3.8 Apply DC to the amplifier.

3.9 Apply a constant TTL **high** signal to the Freq Modulation input on the D-type connector of the RFA741. Connect pin 7 of 'D' to the TTL signal and pin 14 of 'D' to the signal return (0V).

3.10 Apply a constant PLC **high** level (typically 12V or 24V) to the digital gate input on the D-type connector. Connect pin 8 of the 'D' to the Signal and pin 15 of the 'D' to the signal return.

3.11 Apply a constant PLC **low** level (less than 2V) to the POT SELECT input (S0) on the D-type. Connect pin 1 of the 'D' to the Signal and pin 9 of the 'D' to the signal return.
A low level will enable power adjustment using the Manual pots.

Input the laser beam toward the centre of either aperture of the AOM. Ensure the polarization is horizontal with respect to the base and the beam height does not exceed the active aperture height of the AOM. Start with the laser beam normal to the input optical face of the AOM and very slowly rotate the AOM (either direction). See Figure 4 for one possible configuration.



Input Beam Location
Y axis : Centre beam in active aperture height H
X axis : Not critical but avoid clipping device cover

3.12 Observe the diffracted first-order output from the acousto-optic modulator and the undeflected zeroth order beam. Adjust the Bragg angle (rotate the modulator) to maximise first order beam intensity with the 40MHz Frequency selected.

3.13 After Bragg angle has been optimized, slowly increase the RF power by turning PWR ADJ clockwise until maximum first order intensity is obtained.

3.14 The modulator and driver are now ready for use.
When the 50.67MHz is selected, the 40MHz beam will be OFF. A significant proportion of the laser beam will now be diffracted into the 50,67MHz beam location. This will be further from the zero order beam

3.15 Remote RF Power Adjust

The RF power can be adjusted remotely using an I2C compatible interface. The control circuit is based on the Analog Devices non-volatile 256 step digital potentiometer AD5254.
The accompanying data sheet describes the communication protocol.

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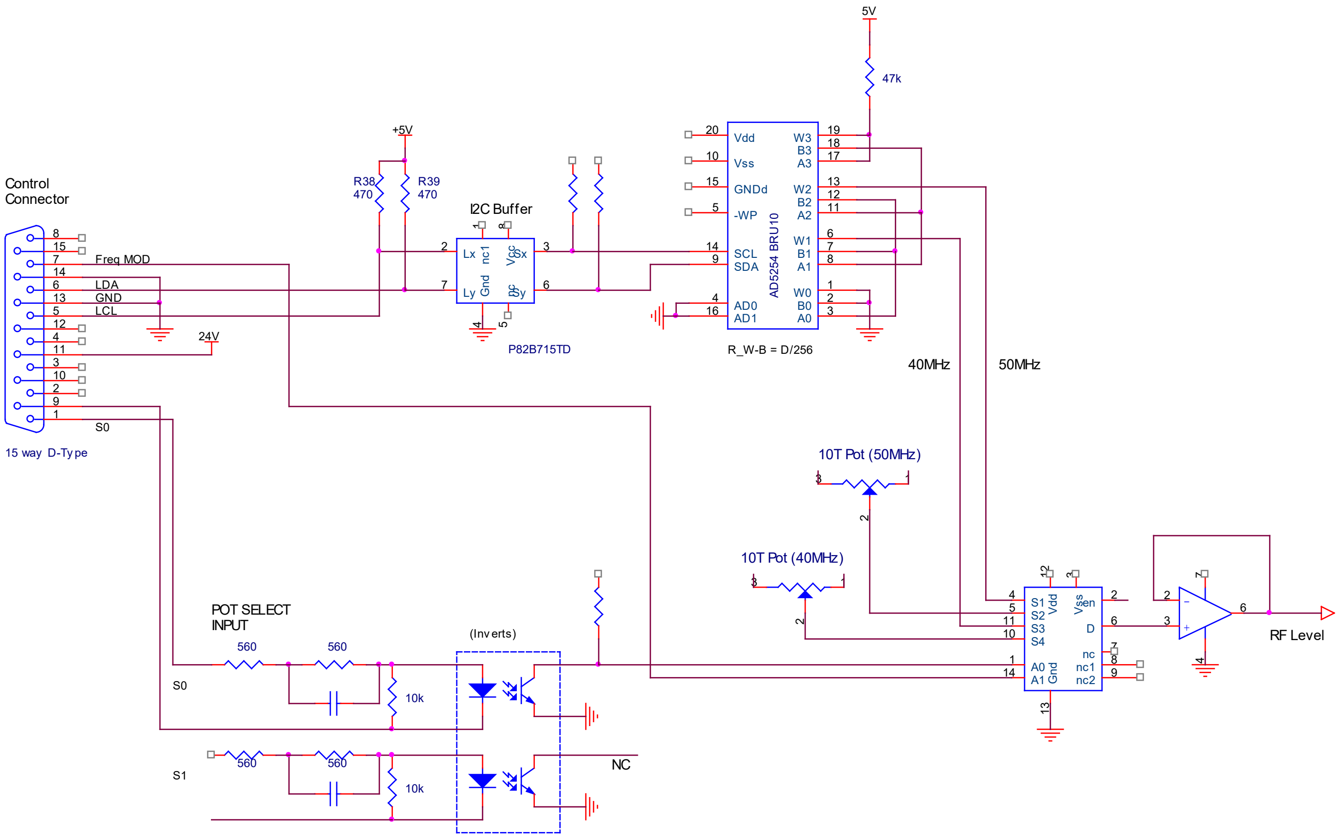
The slave address for the digital I2C potentiometer is at 0101100. (AD0 = AD1 = 0)

Maximum resistance equates to maximum RF power.

The digital potentiometer value is non-volatile and will recall the last saved value on power-up.



DO NOT exceed +5V on the I2C Inputs, LDA (data IO) and LCL (clock)

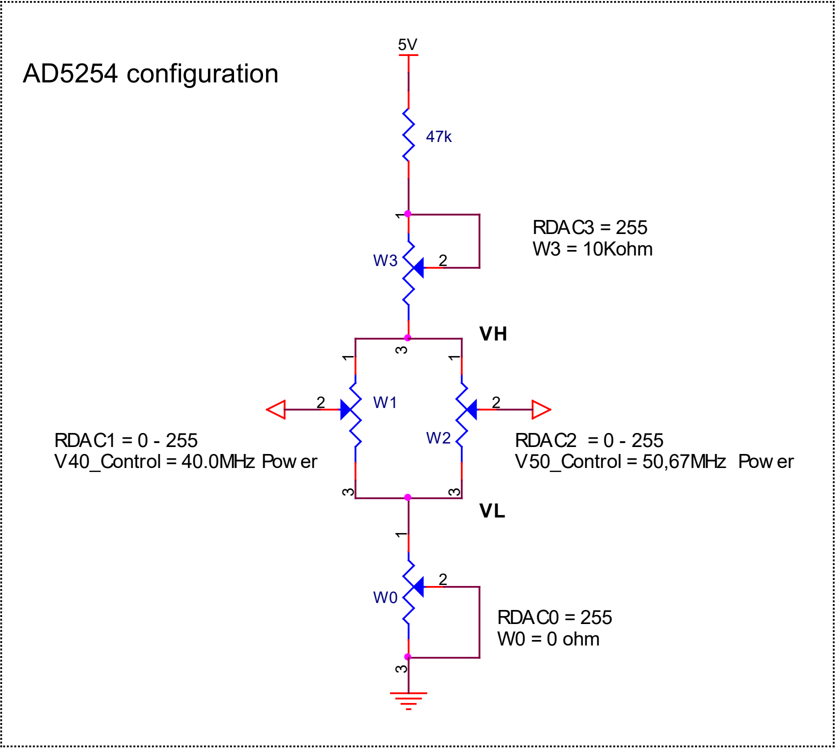
The I2C signals are buffered using the bus extender chip P82B715 from NXP

To enable remote RF power control, connect pin 1 (S0) of the 15way D-type control driver connector to a PLC compatible logic port and apply a high signal.

The four digital pots are configured into a potential divider.

The main power control pots W1 and W2 are in parallel and equate to 5Kohm resistance.

The upper and lower limit adjustment Pots W3 and W0 apply to both 40MHz and 50MHz powers.



RDAC2 defines the 50 MHz power control factor

V50_Control VL + (VH-VL) x W2/255

where W2= 8-bit value programmed into RDAC2

RDAC1 defines the 40 MHz power control factor

V40_Control = VL + (VH-VL) x W1/255

where W1= 8-bit value programmed into RDAC1

RDAC0 defines the lower limit pot

Lower pot resistance R_W0 = (255-W0)/255 x 10Kohm

Lower limit voltage VL = (R_W0) / (47K+R_W3+5K+R_W0)

RDAC3 defines the upper limit pot

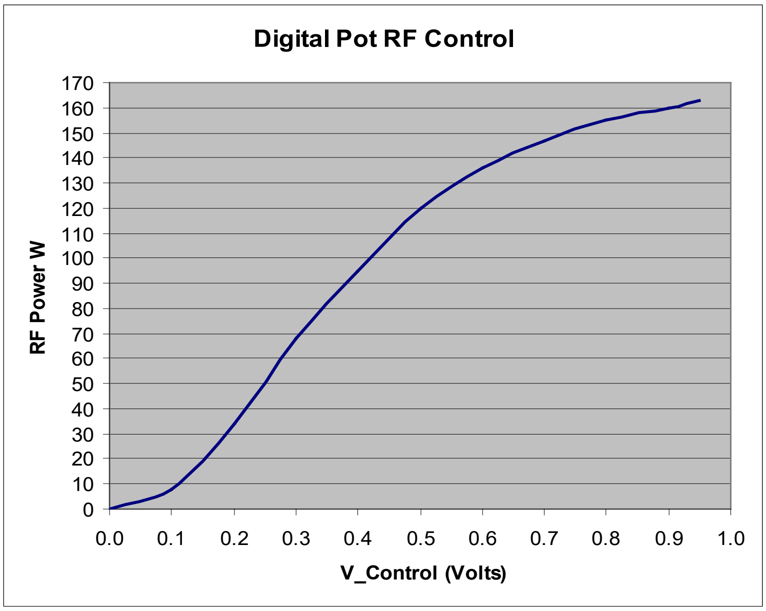
Upper pot resistance R_W3 = (W3)/255 x 10Kohm

Upper limit voltage VH = (R_W0+5K) / (47K+R_W3+5K+R_W0)

The full range power adjustment is shown below.

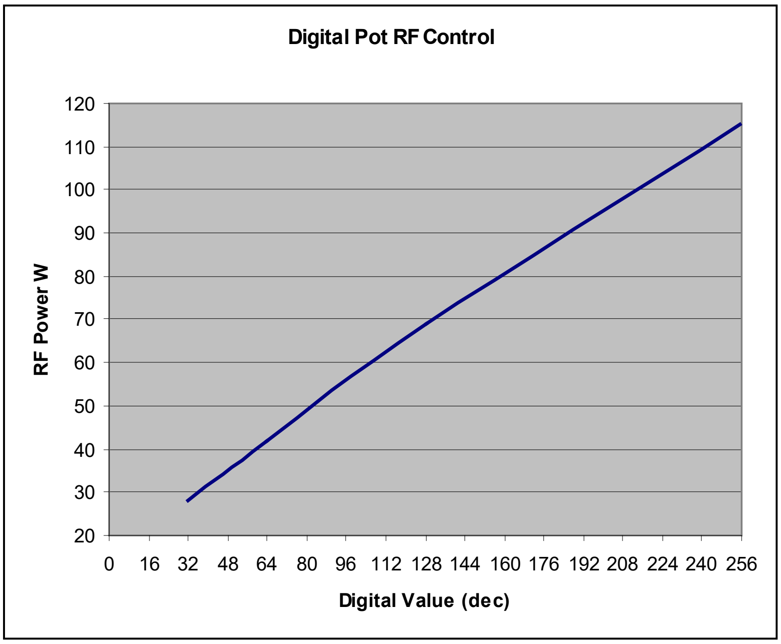
Settings: RDAC3 = 0 (R_W3=0k) and RDAC0 = 255 (R_W0=0k).

The V_Control scale equates to 0 – 255 adjustment range on RDAC1 (W1) or RDAC2 (W2)



By adjusting the values of RDAC0 and RDAC3 it is possible to increase the adjustment resolution of the 8-bit power level control at 40.0 MHz (RDAC1) and 50.7MHz.(RDAC2) over a defined range.

A typical Digital Power curve is shown below. In this case settings are: RDAC3 = 255 (R_W3=10k) and RDAC0 =t 200 (R_W0=2K)



4. MAINTENANCE

4.1 Cleaning

It is of utmost importance that the optical apertures of the deflector optical head be kept clean and free of contamination. When the device is not in use, the apertures may be protected by a covering of masking tape. When in use, frequently clean the apertures with a pressurized jet of filtered, dry air.

It will probably be necessary in time to wipe the coated window surfaces of atmospherically deposited films. Although the coatings are hard and durable, care must be taken to avoid gouging of the surface and leaving residues. It is suggested that the coatings be wiped with a soft ball of brushed (short fibres removed) cotton, slightly moistened with clean alcohol. Before the alcohol has had time to dry on the surface, wipe again with dry cotton in a smooth, continuous stroke. Examine the surface for residue and, if necessary, repeat the cleaning.

4.2 Troubleshooting

No troubleshooting procedures are proposed other than a check of alignment and operating procedure. If difficulties arise, take note of the symptoms and contact the manufacturer.

4.3 Repairs

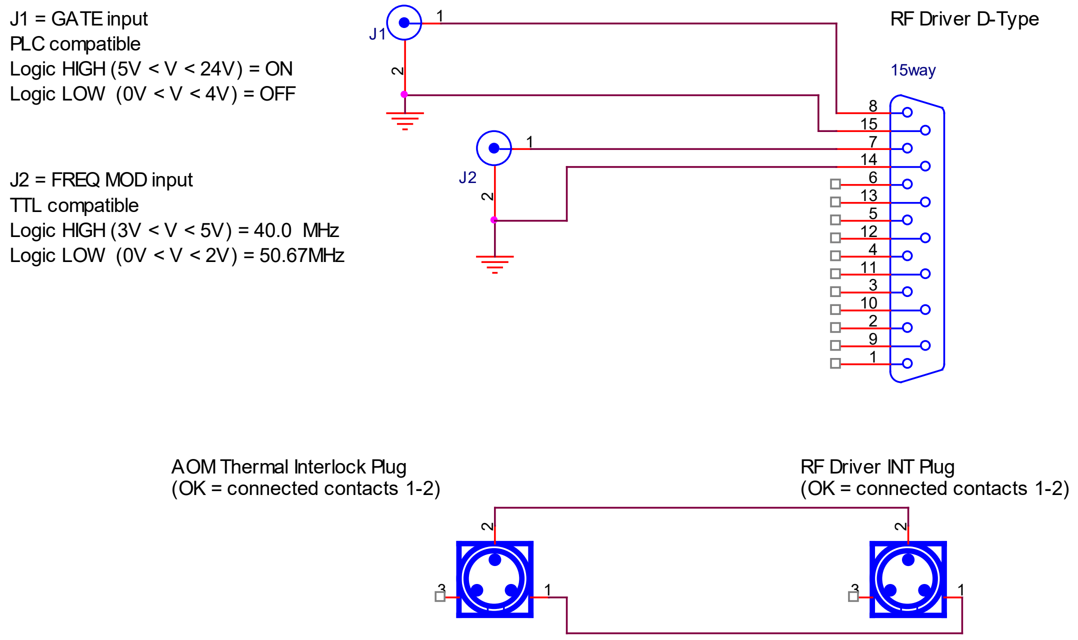
In the event of deflector malfunction, discontinue operation and immediately contact the manufacturer or his representative. Due to the high sensitive of tuning procedures and the possible damage which may result, no user repairs are allowed. Evidence that an attempt has been made to open the optical head will void the manufacturer's warranty.

RFA741 **<u>Connection Summary</u>**

1.0 <u>15 way 'D' Type Control Connection</u>

<u>Signal</u> (see notes)	<u>Type</u>	<u>Pin out connection</u>
NECESSARY		
Digital Gate (slow)** PLC high (5v<V<24v) = ON PLC low (0.0v<V<4v) or NC = OFF	Input	Signal pin 8 Return pin 15
Frequency Modulation (fast)* TTL high (2.7v<V<6.0v) = 40.0MHz TTL low (0.0v<V<0.8v) = 50.67MHz	Input	Signal pin 7 Return pin 14
Interlock *** Normally closed	Input	Connect to AOM "INT"
OPTIONAL		
'Enabled' monitor (Open collector logic, Low = OK) **<u>Maximum applied voltage</u>** **<u>(via external pull up resistor) = 24V</u>** Maximum current = 20mA	Output	Signal pin 2 Return pin 10
'RF Status' monitor (Open collector logic, Low = OK) **<u>Maximum applied voltage</u>** **<u>(via external pull up resistor) = 24V</u>** Maximum current = 20mA	Output	Signal pin 3 Return pin 10
I2C Clock (0.0v<V<5.0v)	Input	Signal pin 5 Return pin 13
I2C Data IO (0.0v<V<5.0v)	In/Out	Signal pin 6 Return pin 13
POT Select Control, S0 PLC high (5v<V<24v) = Digital Pot PLC low (0.0v<V<4v) or NC = Manual Adjust	Input	Signal pin 1 Return pin 9

Modulation and Gate Input connections



Notes:

*** The interlock signal must be connected. Contacts closed for normal operation.

2.0 Mounting Holes

4 x M5

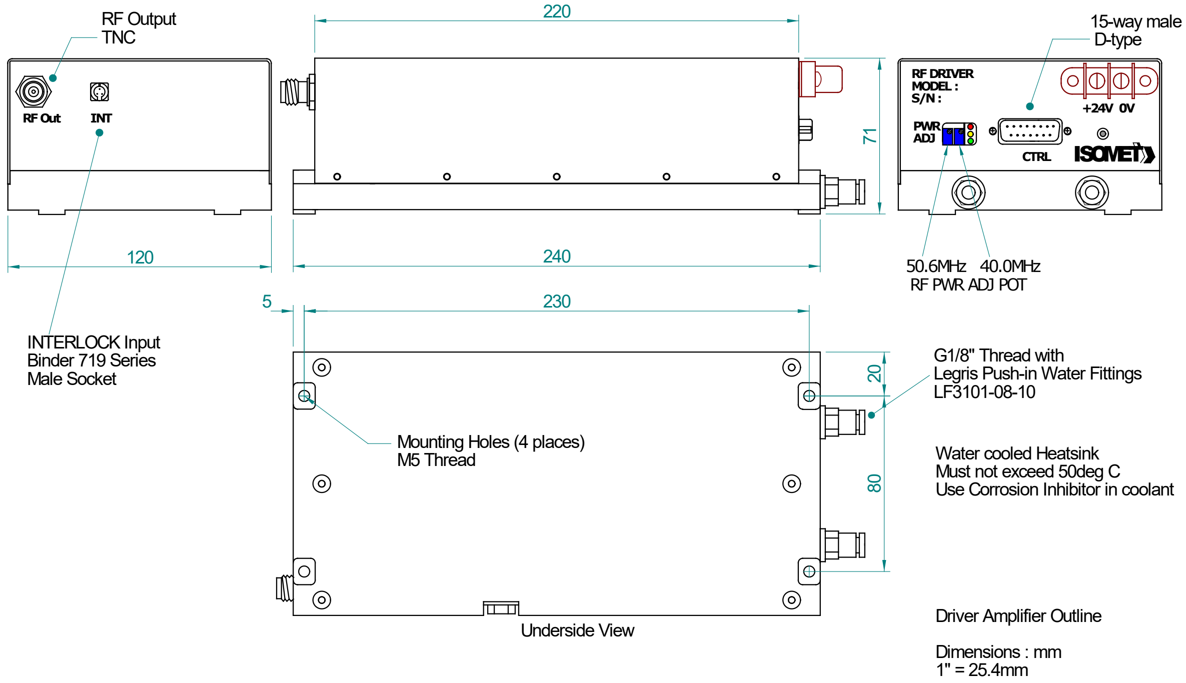


Figure 2: Driver Installation

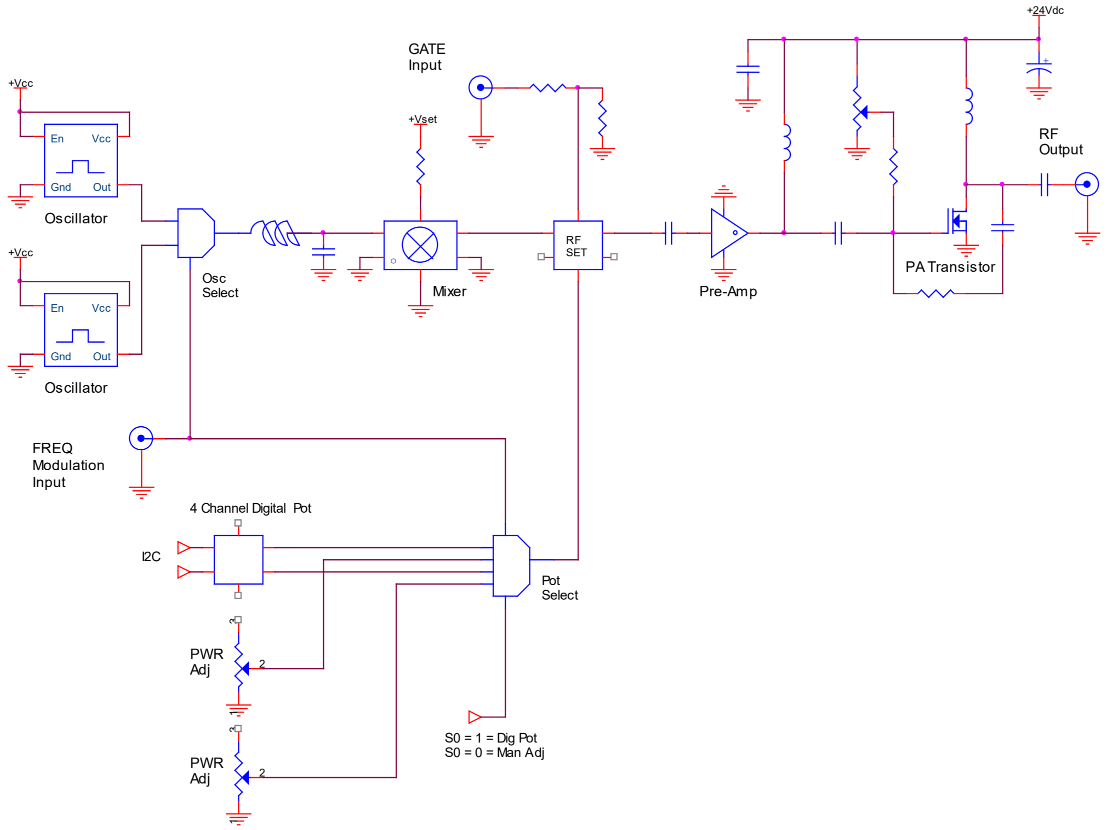
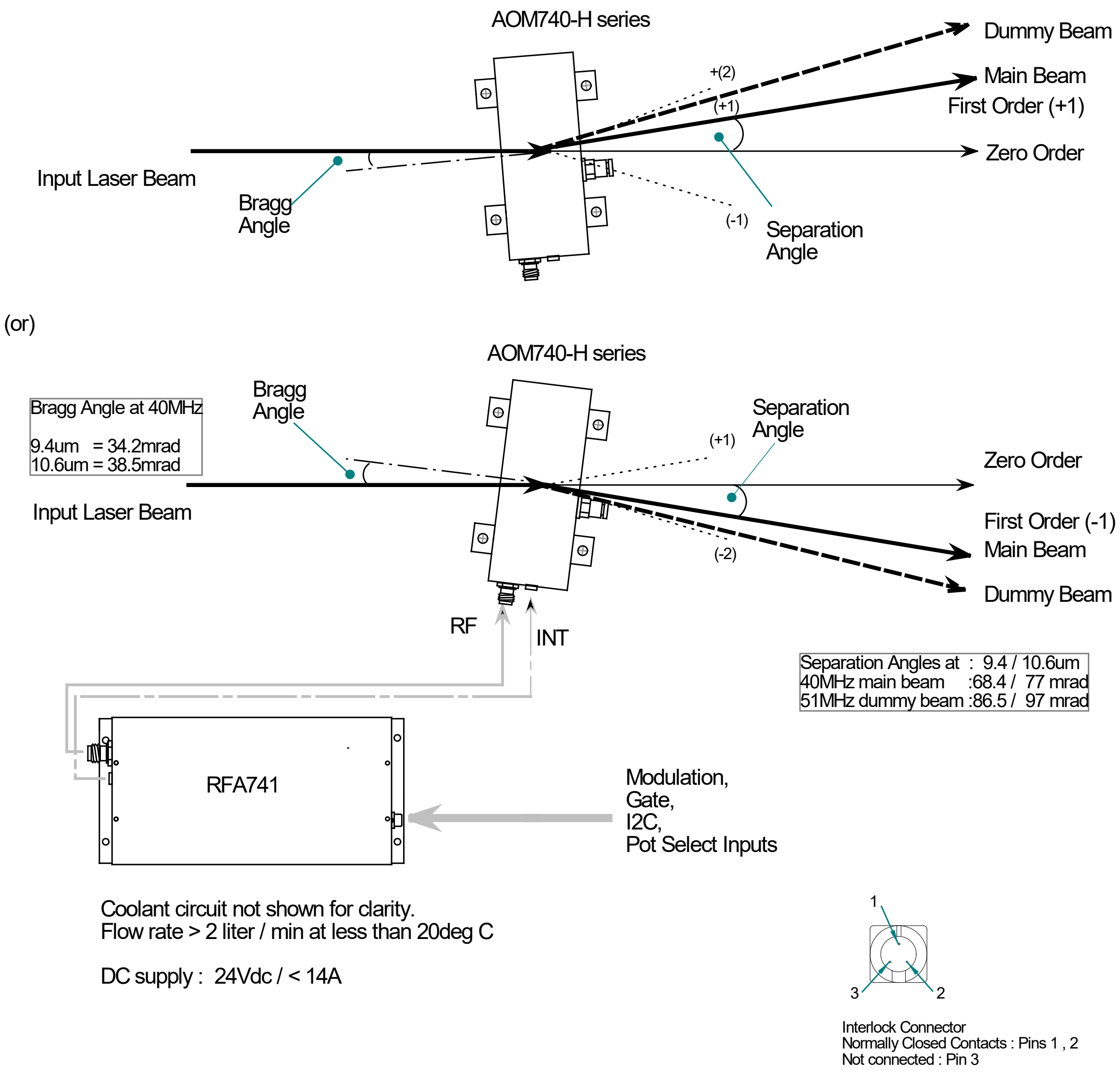


Figure 3: Driver Block Diagram



Either optical face can be used for input.
Thus with reference to the above diagram, the input laser beam can also be from the right to left.

Figure 4: Typical Configurations using RFA741 series.

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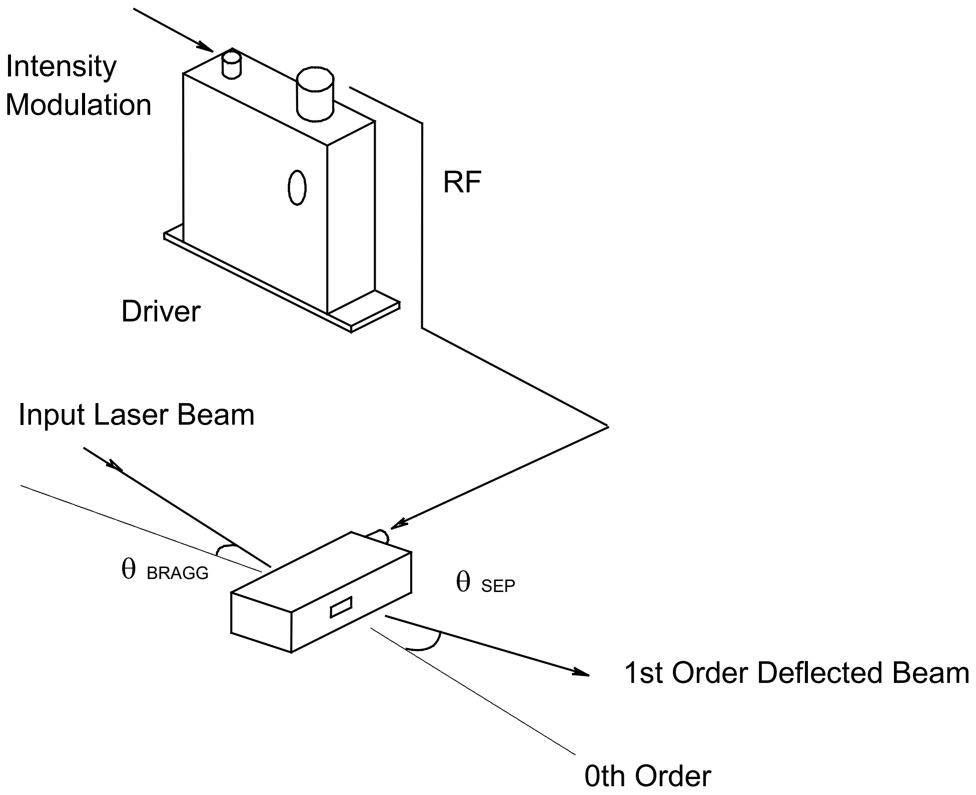
Basic AO Modulator Parameters



The input Bragg angle, relative to a normal to the optical surface and in the plane of deflection is:

$$\theta_{BRAGG} = \frac{\lambda . fc}{2.v}$$

The separation angle between the Zeroth order and the First order is:

$$\theta_{SEP} = \frac{\lambda . fc}{v}$$

Optical rise time for a Gaussian input beam is approximately:

$$t_r = \frac{0.65.d}{v}$$

where:
- λ = wavelength
- fc = centre frequency = 40MHz / 50.67MHz
- v = acoustic velocity of interaction material = 5.5mm/usec (Ge)
- d = $1/e^2$ beam diameter

Figure 5. Modulation System